

VLABS-DEV

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Electronic lock using basic logic gates

Simulation

The diagram shows a logic circuit with four inputs: A, B, C, and D. Inputs A, B, and C are currently 'off' (0), while input D is 'on' (1). The circuit consists of several logic gates: two NOT gates (one for B, one for C), two AND gates (one for A and B', one for A and C'), an OR gate (combining the outputs of the two AND gates), and a final AND gate (combining the output of the OR gate with D). The output is labeled Y = B'D (AC + A'C).

Task: Design a three input electronic lock that operates when A = 1, B = 0, and C = 0. Construct and verify using simulator.

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15/09/2020

Participants (41)

Find a participant

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